Design of a Universal Controller for Distributed Control and Power Electronics Applications

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Abstract—**This paper presents the design of a universal controller for power electronics and distributed digital control applications. The controller interfaces include a dual ring fiber optic interface, a PMC (PCI based mezzanine) interface, a generic pin header interface, an upper level control (ControlNet™) interface, as well as synchronous serial communications interfaces. The controller uses an Analog Devices ADSP-21160 DSP. The controller is multiprocessor capable (self-stacking) and can be configured to work in single processor mode, multiprocessor cluster mode, or multiprocessor data flow mode.**

I. Introduction

In many Power Electronics applications, it is essential to have a digital controller. The development of a digital controller is a time consuming process that generally results in a controller that is specific to a very limited number of power electronics applications. A large amount of time and engineering cost can be saved if a universal controller is available that can satisfy the needs of most medium and high power applications in power electronics.

As part of the Plug and Play effort of the PEBB Program [1], a distributed digital controller was developed [2] that interfaced a DSP to a fiber optic ring. The controller controlled three smart phase legs (referred to in [2] as hardware managers) of a 100kW voltage source inverter. Each phase leg was an independent node on the fiber optic ring. Space vector modulation or 3-phase sinusoidal PWM was implemented in the DSP, and the resulting duty cycles were sent through the fiber optic ring to the phase legs. The phase legs in turn returned information such as the phase current. Using fiber allowed for no EMI problems.

The controller described above is implemented on a board provided by Bittware Research Systems. While this board is suitable for performing the operations described above, there is a need for a board more specific to the needs of a distributed controller.

A new controller is proposed here that implements several features desirable to high power and medium power applications such as redundant communication, upper level interfaces, and debugging tools. This controller maintains the features of and is backwards compatible with the previous controller.

This universal controller will be able integrate into the current systems at CPES with minimal overhead. CPES has developed several other converters that use this previous controller such as a multi-level converter used to control a SMES (Super magnetic Energy Storage) system, a four-leg inverter, a PFC boost rectifier, and a matrix converter.

This controller makes available several interfaces such as a PCI compliant interface called PMC, and a factory automation interface, ControlNet. The controller has a synchronous serial port interface (SPI), and a link port, which transfers data one byte at a time and is available on several DSPs produced by Analog Devices.

II. Controller Architecture

The controller contains two main busses. One bus allows for multiple DSP support via a self-stacking connector while the other bus interfaces peripherals and upper level communication interfaces necessary for supervisory control systems, monitoring and debugging utilities to interface with the controller. There is a bridge between the two busses that is implemented by an FPGA. Both busses have expansion connectors so that more devices can be added to the peripheral bus and more Universal Controllers can be added to the system, increasing the processing power of the controller by combining the power of several controllers into one.

Additional features on the controller include an EEPROM for debugging, logging, and parameter storage, a hex display, which is good for indicating fault conditions, status, and debugging, and an analog to digital converter that lets users debug their DSP code. The controller architecture is shown in figure 1.

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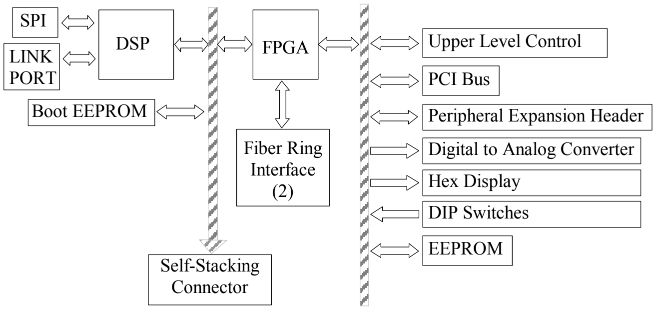

Fig. 1 Universal Controller Architecture

III. DSP SELECTION AND FEATURES

One desired capability of the DSP is that it be easy to port code from the existing DSP used in [2] to the new DSP. The DSP previously used is Analog Devices ADSP-21062. For the new DSP, the ADSP-21160 has been chosen. This DSP has several features that will benefit the new Universal Controller.

The ADSP-21160 has built-in support for multiprocessor applications. This DSP has on-chip bus arbitration. The DSP can work in parallel with up to six other ADSP-21160s. These DSPs can be configured to share external memory or can access each other's memory and processor resources via direct memory access (DMA). Since this Universal Controller will contain one DSP and one FPGA, in order to create a multiprocessor system, the controller will be self-stacking to allow for multiple Universal Controllers to be combined, creating a more capable controller. Using this method, any DSP on the controller can access any other DSP or FPGA, giving it access to the entire controller. This is beneficial when there are different peripherals or networks connected to the different FPGAs.

The ADSP-21160 also has a built-in DMA controller that supports up to 14 DMA channels. Other resources on the Universal Controller can be accessed via DMA, such as the PCI interface chip and other DSPs in a multiprocessor environment.

One drawback of many DSPs is the limited amount of memory that is available to the user. The ADSP-21160 has 4 MBits of Dual-Ported RAM on board, which is usable as program memory or data memory. In addition, the DSP supports SDRAM, allowing for up to 4 GWords of addressable memory. In this Universal Controller, additional memory is made accessible via a mezzanine card that is placed on the multiprocessor bus via the self-stacking connector. This memory can be shared across all DSPs when several boards are stacked together.

The processor also allows communication via link ports. Each link port can transfer 100 Mbytes per second. These can also be used to connect several controllers to form a multiprocessor system. This type of multiprocessor system has independent memory, unlike the cluster multiprocessing method, where all of the memory and resources are shared between processors. This method can be combined with the cluster multiprocessing method described above to create a larger system if necessary. The link ports can also be used as a way to boot the processor.

The DSP also has a built-in synchronous serial communication interface (SPI). This interface can be used to communicate with other processors, Universal Controllers, or peripheral devices that support synchronous serial communication.

The ADSP-21160 supports Single Instruction Multiple Data (SIMD) operations via two processing elements (PE). There are three elements within each PE in this DSP. They are a barrel shifter, a multiplier, and an ALU. Within each PE, these three can be operated in parallel, which allows for the processor to operate at a maximum of 600 MFLOPS.

Finally, the DSP supports emulation and programming via a JTAG interface. This is convenient for development and debugging. Using the JTAG interface with the emulator, it is possible to run the code on the DSP while debugging it from a PC.

IV. FIBER OPTIC RING INTERFACE

In the previous version of the Universal Controller, the fiber optic ring interface was provided by two TAXI chips from AMD (AM7968 and AM7969). One chip was the receiver, and the other chip was the transmitter. This fiber optic ring interface is shown in figure 2.

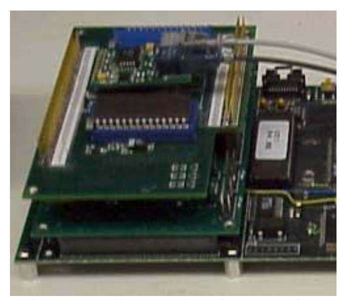
Figure 2: Fiber Optic Ring Interface

Cypress has combined the functionality of the two TAXI chips into one chip, Cypress CY7C9689. The new chip contains both the transmitter and receiver in a 100-pin TQFP package. The CY7C9689 is pin compatible with the previous AMD TAXI chips. The new Universal Controller will use this chip. This chip supports communication over fiber at a rate of 200 MBaud.

This controller will support two of these transceivers. This will allow the application to support two individual fiber optic rings or one redundant ring, which improves the reliability of the distributed application.

These two transceivers are connected to the Universal Controller via the FPGA. The FPGA will present the transceivers to the DSP as memory locations. Since the user can control what the FPGA will do by changing the underlying VHDL code, it is possible to implement the protocol and any redundancy in the FPGA, while providing the DSP with an interface similar to Dual-Ported RAM. This way, the DSP does not have to encapsulate the information into a packet, which gives it more time to deal with application specific issues as opposed to communication overhead.

The fiber optic ring interface code in the FPGA will be designed to implement a protocol called PESNet [5]. This protocol was developed as a way for different elements of a power electronics system to communicate with each other.

V. PMC INTERFACE

PCI-Mezzanine (PMC) is an interface that is PCI compliant but connects to the host as a mezzanine card. This allows for the card to be connected to other PCI cards or VME cards that have PMC interfaces on them. Several companies make PMC host carrier cards. One of these cards is shown in figure 3.

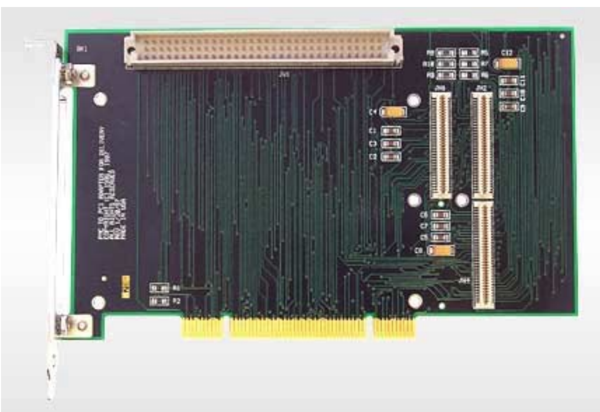

Figure 3: PMC Host Board

By using this card, the Universal Controller can be present on either a PCI bus or a VME bus. This way, those who want to use a PC to do development can connect the Universal Controller to their PC via PCI, and those who want to install the Universal Controller into a VME chassis can do that also.

Since the PMC logical interface is the same as the PCI logical interface, the Universal Controller will use a PCI interface chip provided by Cypress. The Cypress CY7C09449PV-AC is a PCI interface chip that makes use of Dual-Ported RAM and an I^2C interface. This simplifies the chip initialization. If the initialization is constant, then the parameters can be stored in an EEPROM, and the I^2C bus can be used to initialize the chip from the EEPROM via the FPGA.

This PCI interface chip will be connected to the peripheral interface bus and will communicate with the DSP using the lower 32 bits of the DSP's 64-bit data bus.

This interface lets the Universal Controller to communicate with the PC during runtime. This method would allow some of the control code to be implemented on the PC in another program. Companies such as DSpace have done this with their controller cards using RealTime Workshop™ from MathWorks, which allows Matlab to interact with the DSP during runtime.

Other uses of this interface include runtime monitoring of the fiber-optic rings and data busses, as well as hardware emulation.

Hardware emulation allows the Universal Controller to appear on the fiber optic ring as another piece of hardware. This is useful for simulating fault conditions that may be difficult to produce on the real hardware. Another use of hardware emulation is to make one Universal Controller appear as a PEBB (Power Electronics Building Block) or other element on the fiber optic ring that is still under development. If the Universal Controller can simulate the behavior of the new hardware before the new hardware is completed, then the control code for the system can be developed in parallel with the new hardware, which can save development time.

Runtime monitoring is useful for logging data and debugging the system. It is possible to read the data destined for another device on the fiber optic ring and report that data to some program running on the PC. This can be useful for debugging purposes when developing a new PEBB. It is also useful when one wishes to monitor the variables in the system that are communicated over the fiber ring. If the Universal Controller is connected to the PC, then it can monitor parameters in a process or in a phase leg such as some temperature or current. If a temperature is too high, for example, a program running on the PC can set some alarm or notify some user.

VI. UPPER LEVEL COMMUNICATION INTERFACE

It is rare that a converter or process will be operated without some form of supervisory control. Several vendors have created fieldbusses that are designed for industrial process control. Devices such as motor drives, digital and analog I/O and PLCs exist on such busses. These interfaces will be referred to as upper level communication interfaces.

Since it is impossible to predict what the end user will use as their upper level communication interface, a header is provided on the Universal Controller so that the end user can provide a piggyback card that will implement the upper level interface that they are using. The piggyback card should present the upper level interface as Dual-Ported RAM.

Several options were explored for this interface, including Profibus, DeviceNet, ControlNet, and Ethernet. Although any interface can be chosen and implemented, we will implement one example interface using ControlNet. ControlNet operates at 5 MBaud and provides redundant communication links over either copper or fiber. The protocol is also compatible with other fieldbus protocols such as Foundation Fieldbus and DeviceNet.

Allen-Bradley provides an ASIC that implements the ControlNet protocol. That ASIC is the CNA10M. The chip has two onboard communications processors to implement the protocol. An EEPROM will contain the firmware (provided by Allen-Bradley) for this chip.

Since different busses have different physical interfaces, it is impossible to place the connectors for this interface on the main controller board. Therefore, it is necessary to place the physical connectors to the fieldbus on the piggyback card also.

In addition to performing a slave-like role in these interfaces, the Universal Controller may also utilize devices on these upper level interfaces as its own slaves (depending on the protocol). Some protocols allow for multi-master environments where this may be possible. This method would allow for additional I/O and capabilities to be added to the Universal Controller that already exist in industry. This saves development cost. In addition to these devices, it may also be possible to place another Universal Controller on this bus, which would allow the two Universal Controllers to communicate over the fieldbus.

This interface, like the PMC interface may also be used to monitor the status of devices on the fiber optic ring for debugging or monitoring and safety purposes.

VII. Peripheral Expansion Header

Several converters were developed in CPES that make use of two boards that were connected to the previous Universal Controller. One of these boards is an analog interface board which contained analog to digital converters and buffers. The other board is a digital interface board used to control gates and monitor fault signals. These two boards were connected to the Universal Controller via an EPLD interface board. The two analog and digital boards are shown in figure 4. The board on the bottom is the previous Universal Controller board. The board on the top left is a digital interface board. The board on the top right is the analog interface board.

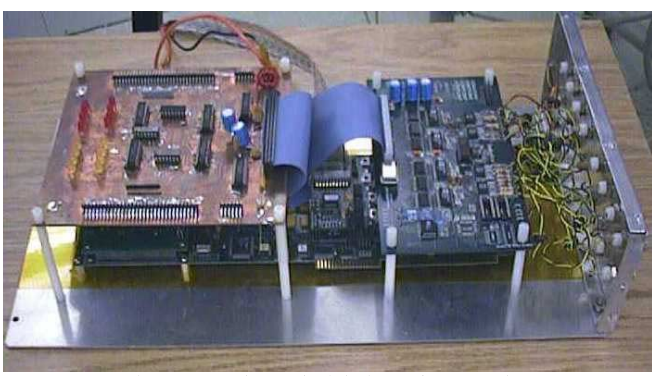

Figure 4: Analog and Digital Interface Boards

The new Universal Controller will have interfaces that will allow the analog and digital boards to be directly connected to the Universal Controller. The code that was previously done in the EPLD will be done in the FPGA. This way, the boards that were developed previously can still be used with the new controller. This interface is not restricted to these two boards. If a new board is developed, it will be possible to interface that new board to the Universal Controller through this interface. This way, it is possible to expand the universal controller in another way to add capabilities that are specific to the needs of an application. Many of these pins are directly connected to dedicated pins on the FPGA. The user can modify the VHDL code in the FPGA to customize the behavior of these pins to their application.

VIII. Conclusion

A Universal Controller architecture has been described that further enhances the capabilities of the existing controller. Controller applications and peripherals have been described, and the controller expansion methods have been discussed.

Eventually, this converter may run an operating system for power electronics applications with modularized control objects referred to in [6] as ECOs.

The controller will be implemented in the CPES lab at Virginia Tech for controlling PEBB modules in medium to high power PEBB based converters.

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