
Tasks

Project: PEBB Plug and Play

Assigned To Daniel Ghizoni

T#45

Opened 6/7/2002 10:19:40 AM

Status InProgress

Closed

Category Universal Controller

Assigned By Jerry Francis

Summary Take inventory and make database for UC

Description We need to make a database of the inventory that we have to determine if we need to order anything. We can use this same database to generate a BOM for the assembly house.

Comments

Assigned To Gasha Gataric

T#24

Opened 2/28/2002 3:12:01 PM

Status Canceled

Closed

Category Universal Controller

Assigned By Jerry Francis

Summary Reorder power planes

Description (General Dynamics:) Need to reorder power planes so that the 2.5 volt plane is in the middle, close to the ground plane. This will reduce the warpage.

Comments Jerry Francis, 6/7/2002, (48): We are not going to do this.

T#25

Opened 2/28/2002 3:12:59 PM

Status InProgress

Closed

Category Universal Controller

Assigned By Jerry Francis

Summary Need to redo bypass capacitor connections

Description (General Dynamics:) Bypass capacitors need to be directly connected to the ground plane and the power plane, and not using a trace to connect to the device.

Comments

T#22

Opened 2/26/2002 11:32:41 AM

Status Open

Closed

Category Universal Controller

Assigned By Jerry Francis

Summary PMC RDYIN\ is not connected to anything

Description The PCI interface chip, CY7C09449PV-AC has a RDYIN\ pin that needs to be tied low. Need to connect RDYIN\ to ground and RDYIN to VCC as shown in the cypress application notes.

Comments Jerry Francis, 6/7/2002, (49): Fixed schematic.

T#28

Opened 3/5/2002 8:29:54 AM

Status Open

Closed

Category Universal Controller

Assigned By Jerry Francis

Summary PMC Holes are off

Description (General Dynamics:) The PMC holes are still off by less than 1/8 of an inch. Holes need to be moved.

Comments

	T#33	<i>Opened</i> 4/25/2002 10:38:11 AM
<i>Status</i>	Open	<i>Closed</i>
<i>Category</i>	Universal Controller	<i>Assigned By</i> Jerry Francis
<i>Summary</i>	Socket the boot flash	
<i>Description</i>	Need to socket the boot flash. See http://www.emulation.com/ . They have one for less than \$20.	
<i>Comments</i>	Jerry Francis, 6/7/2002, (47): Also make sure that there is enough room on the PCB for the socket, as it is bigger than the part. Look for the PMC holes to ensure that they are ok. The part number is S-TSO-SM-032-A1.	
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	T#17	<i>Opened</i> 2/26/2002 11:22:55 AM
<i>Status</i>	Resolved	<i>Closed</i>
<i>Category</i>	Universal Controller	<i>Assigned By</i> Jerry Francis
<i>Summary</i>	Need to fix power connection to common mode choke	
<i>Description</i>	The input connector to the controller goes directly to the power plane instead of passing through the common mode choke. Need to fix this on the power page before the next board run.	
<i>Comments</i>	Jerry Francis, 6/7/2002, (52): Fixed. Schematic. Removed ground power symbol that was connecting the input connector to the ground plane.	
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	T#18	<i>Opened</i> 2/26/2002 11:23:57 AM
<i>Status</i>	Resolved	<i>Closed</i>
<i>Category</i>	Universal Controller	<i>Assigned By</i> Jerry Francis
<i>Summary</i>	HEX Display input lines are not in correct order	
<i>Description</i>	The input lines to the HEX displays are in the wrong order. Check the datasheet to see the correct pinout for the data lines.	
<i>Comments</i>	Jerry Francis, 6:07:02 AM, (51): Fixed on schematic. Jerry Francis, 3/8/2002, (30): A temporary fix has been made in the VHDL to swap the bits into the correct order. The HEX code will work correctly for now.	
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T#19 *Opened* 2/26/2002 11:25:25 AM
Status Resolved *Closed*
Category Universal Controller *Assigned By* Jerry Francis
Summary FPGA clock does not go to multilinx connector
Description The FPGA clock does not go to the multilinx connector. The clock net is called CCLK. The net label on the connector is FPGACLK. This needs to be changed to CCLK. Also add a series or parallel termination resistor.
Comments Jerry Francis, 6:07:02 AM, (50): Fixed on schematic.

T#37 *Opened* 4/29/2002 9:42:06 AM
Status Resolved *Closed*
Category Universal Controller *Assigned By* Jerry Francis
Summary JTAG connector is mirrored
Description The JTAG connector is mirrored on the board. We need to fix this.
Comments Jerry Francis, 6/7/2002, (54): Mirrored JTAG connector in library so that it is correct.

Assigned To Jerry Francis

T#34

Opened 4/25/2002 10:40:32 AM

Status Canceled

Closed

Category Universal Controller

Assigned By Jerry Francis

Summary Need to move LEDs so they are visible from front

Description When the card is installed in a VME rack, the power leds should be visible from the front panel.

Comments Jerry Francis, 6/7/2002, (46): Not an issue

T#39

Opened 4/29/2002 9:44:15 AM

Status Canceled

Closed

Category Universal Controller

Assigned By Jerry Francis

Summary Need to make HEX displays visible from front panel

Description We need to make the HEX LEDs visible from the front panel. Consider stacking distance. Also consider the orientation in the VME chassis to avoid upside down numbers. May need a 90 degree mounting connector.

Comments Jerry Francis, 6/7/2002, (42): Do not need to do this.

T#8

Opened 2/25/2002 4:29:02 PM

Status Closed

Closed 3/19/2002

Category Universal Controller

Assigned By Jerry Francis

Summary PROM Does not program FPGA

Description When the PROM tries to program the FPGA, it appears to do it in serial mode instead of parallel mode, regardless of which option is selected when the Multilinx Cable is programmed. Call Xilinx and get a support case on this.

Comments Jerry Francis, 2/28/2002, (17): Made a Xilinx webcase. The webcase ID is 412854. The Contact ID is 151078. The site ID is 3199.

Jerry Francis, 3/19/2002, (34): The problem was in the programming software. Xilinx iMPACT does not set the parallel bit. JTAG programmer does. See ftp://customer.xilinx.com/download/jtag_programmer.exe to get the tool that can program it. Set to closed.

T#10 *Opened* 2/25/2002 4:37:21 PM
Status Closed *Closed*
Category Universal Controller *Assigned By* Jerry Francis
Summary Wake up the DSP
Description (From General Dynamics) Need to activate the DSP and see if we can download a simple program to it in VHDL.
Comments Jerry Francis, 2/26/2002, (13): Need to add to the constraints file.
Jerry Francis, 2/28/2002, (18): Added VHDL code to try to wake up the DSP. We haven't been able to do it successfully yet. It seems that the receive clock is not running. I will try to use the CCLK as an input and see if that works.
Jerry Francis, 3/7/2002, (25): I was able to see the reset sequence in the DSP, but was unable to verify that the DSP is working yet. I removed R106 and wired to R115. This solution fixes the problem of the Fiber receive clocks not running without data.
Jerry Francis, 4/29/2002, (37): I was able to wake up the DSP and execute code using the emulator. We need to test the connections between the DSP and the FPGA.
Jerry Francis, 6/7/2002, (53): We can program the DSP without a problem.

T#21 *Opened* 2/26/2002 11:31:19 AM
Status Closed *Closed*
Category Universal Controller *Assigned By* Jerry Francis
Summary Need to buy an emulator
Description We need to buy an emulator that supports the ADSP-21160 DSP
Comments Jerry Francis, 2/24/2002, (36): Done. We have an emulator - ADDS-SUMMIT-ICE pci based emulator.
Jerry Francis, 2/28/2002, (21): Waiting on money.

	T#23	<i>Opened</i> 2/26/2002 11:35:27 AM
<i>Status</i>	Closed	<i>Closed</i>
<i>Category</i>	Universal Controller	<i>Assigned By</i> Jerry Francis
<i>Summary</i>	Purchase BGA debugging assembly	
<i>Description</i>	(From General Dynamics). Need to purchase a BGA debugging assembly to mount on the board, and place it on one of the new boards. See Emulation Technologies. See the following link. http://www.emulation.com/catalog/off-the-shelf_solutions/logic_analyzer-scope_adapters/surface_mountable_bug_katchers/bga/	
<i>Comments</i>	Jerry Francis, 2/28/2002, (22): waiting on money Jerry Francis, 4/25/2002, (35): This has been overcome by events. Setting to closed. The peripheral pins seem to work good enough so that we do not need to break out the pins on the bga.	
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	T#29	<i>Opened</i> 3/1/2002 8:16:57 AM
<i>Status</i>	Closed	<i>Closed</i> 3/7/2002
<i>Category</i>	Universal Controller	<i>Assigned By</i> Jerry Francis
<i>Summary</i>	Fix U26	
<i>Description</i>	U26 came off the board. We need to put it back.	
<i>Comments</i>	Jerry Francis, 3/1/2002, (27): Ordered samples to fix board. Jerry Francis, 3/7/2002, (28): Board fixed. New device is on board and is working.	
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	T#30	<i>Opened</i> 3/8/2002 8:27:43 AM
<i>Status</i>	Closed	<i>Closed</i> 3/8/2002
<i>Category</i>	Universal Controller	<i>Assigned By</i> Jerry Francis
<i>Summary</i>	Deliver testplan to General Dynamics	
<i>Description</i>	Universal controller testplan with updated memory map needs to be sent to General Dynamics.	
<i>Comments</i>		
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	T#38	<i>Opened</i> 4/29/2002 9:43:06 AM
<i>Status</i>	Closed	<i>Closed</i>
<i>Category</i>	Universal Controller	<i>Assigned By</i> Jerry Francis
<i>Summary</i>	Need to determine material to make new board from	
<i>Description</i>	We need to find the correct material to use to make a new board. Also consider material thickness and supplier.	
<i>Comments</i>	Jerry Francis, 6/7/2002, (43): We will keep using the same material and thickness.	

	T#13	<i>Opened</i> 2/25/2002 4:58:12 PM
<i>Status</i>	InProgress	<i>Closed</i>
<i>Category</i>	Universal Controller	<i>Assigned By</i> Jerry Francis
<i>Summary</i>	Need to consider building more boards for GD-AIS	
<i>Description</i>	(General Dynamics, 2/22/02 meeting: We need to provide General Dynamics with a new board soon so that they can also use the universal controller. Should they take ours? When do we need to produce more boards?	
<i>Comments</i>	Jerry Francis, 4/29/2002, (39): We will produce more boards. A list has been sent to Gasha to see what changes he can make fast.	
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	T#16	<i>Opened</i> 2/26/2002 11:20:30 AM
<i>Status</i>	InProgress	<i>Closed</i>
<i>Category</i>	Universal Controller	<i>Assigned By</i> Jerry Francis
<i>Summary</i>	Make complete constraints file	
<i>Description</i>	Need to create the complete constraints file. Unused pins will go to a logic constant. We need to avoid this and write 'Z' to the unused ones. Use the schematic.	
<i>Comments</i>	Jerry Francis, 2/28/2002, (20): Added the DSP pins to the constraints file that are used for waking it up. We need to add more as we start using them and they appear in the constraints editor.	
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	T#46	<i>Opened</i> 6/11/2002 10:23:03 AM
<i>Status</i>	InProgress	<i>Closed</i>
<i>Category</i>	Universal Controller	<i>Assigned By</i> Jerry Francis
<i>Summary</i>	FPGAWRITE needs pulldown	
<i>Description</i>	The FPGA write signal needs a pulldown resistor	
<i>Comments</i>		
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	T#26	<i>Opened</i> 3/1/2002 11:17:15 AM
<i>Status</i>	Open	<i>Closed</i>
<i>Category</i>	PESNet Protocol	<i>Assigned By</i> Xiangfei Ma
<i>Summary</i>	Talk with steve about Workview Office	
<i>Description</i>	We need to ensure that we have some VHDL simulation tool available on the workstation lab computers.	
<i>Comments</i>	Jerry Francis, 3/8/2002, (29): I will see about getting workview office available. I believe that synopsys is also available, but I don't know how to use it well.	
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T#32 *Opened* 3/19/2002 9:12:08 AM
Status Open *Closed*
Category Universal Controller *Assigned By* Jerry Francis
Summary Add silkscreen labels to dip switches
Description J11 and J12 do not have labels on the DIP switches to indicate what they mean. J8, J7, and J5 also need functional labels. Same for J17.

Comments

T#35 *Opened* 4/29/2002 9:40:14 AM
Status Open *Closed*
Category Universal Controller *Assigned By* Jerry Francis
Summary Move the reset button to the front
Description Need to move the reset button to the front of the panel so that it is accessible from a front panel.
Comments Jerry Francis, 6/7/2002, (45): The reset button should be moved to the other side of the board atleast.

T#42 *Opened* 6/3/2002 10:01:36 AM
Status Open *Closed*
Category Universal Controller *Assigned By* Jerry Francis
Summary DACLDB not connected
Description DACLDB not connected to pin on FPGA. There is a small space between the wire and the schematic symbol. Need to fix before next release.

Comments

T#36 *Opened* 4/29/2002 9:41:16 AM
Status Resolved *Closed*
Category Universal Controller *Assigned By* Jerry Francis
Summary Move JTAG connector to the front
Description Need to move the DSP JTAG connector to the front so that it is accessible from a front panel
Comments Jerry Francis, 6/7/2002, (44): Made DSP connector a socket that does not extend past board extents. Fixed problem without having to move connector.

T#40 *Opened* 4/29/2002 9:46:50 AM
Status Resolved *Closed*
Category Universal Controller *Assigned By* Jerry Francis
Summary Investigate clocking scheme
Description Related to T#10. We need to determine how to manage the clocks during powerup reset. Also look at clock skew issue. Work with GDDS.
Comments Jerry Francis, 6/7/2002, (41): Updated schematic so that FPGA feeds from cluster clock and not DSP clock.

T#41 *Opened* 5/14/2002 11:01:06 AM
Status Resolved *Closed*
Category Universal Controller *Assigned By* Jerry Francis
Summary User DIP Switches
Description The user dip switches (lowest two bits) do not appear to work with the DSP. This problem could be in VHDL or in the hardware. Most likely, it is hardware.
Comments Jerry Francis, 6/7/2002, (40): Fixed in VHDL. The data was not being latched, and was disappearing before the DSP could grab it.

Assigned To Jinghong Guo

T#14

Opened 2/25/2002 5:00:25 PM

Status InProgress

Closed

Category PESNet Protocol

Assigned By Stephen Edwards

Summary Need a design example for PESNet

Description We need a benchmark example for PESNet. Some control topologies that are representative of a challenging application. Consider Bettis example and Virginia Tech Proposal to ONR Task 3 for PnP.

Comments

Assigned To Luca Solero

T#15

Opened 2/25/2002 5:02:05 PM

Status InProgress

Closed

Category Hardware Manager

Assigned By Dushan Boroyevich

Summary Need to start hardware manager architecture

Description We need to produce hardware managers that can be used as part of new phase legs. We need to select the architecture for both the digital and power stage boards. We need to select components such as FPGAs, connectors, DC/DC converters and such.

Comments

Assigned To Xiangfei Ma

T#31

Opened 3/8/2002 4:28:08 PM

Status InProgress

Closed

Category PESNet Protocol

Assigned By Stephen Edwards

Summary Investigate using another transceiver

Description AMD produced the original TAXI chips. They now stopped producing them, and so we used the Cypress chips for Hotlink (TAXI). However, it seems that the TAXI chips are going out of style. It is a good idea to move to a standardized protocol at this level. Investigate the possibility of using something else instead that is more standardized. Determine what compatibility issues there will be and how easy it will be to fix them.

Comments Jerry Francis, 3/8/2002, (31): Consider using SONET OC-3 / UTOPIA. UTOPIA uses 8B/10B encoding. We can manage this in the controller easily using the current cypress chips and bypassing the 4B/5B encoder and implementing the 8B/10B in the FPGA as a pipeline stage. The frequency is also different (155 Mbaud) and the wavelength is different (1310nm). We should ensure that plastic fiber is suitable. If not, then try Hard-Clad silica or another alternative (glass will work too, but has disadvantages of cost and being fragile.). I ordered some optical transceivers from Infineon to evaluate its use.

T#9

Opened 2/25/2002 4:32:06 PM

Status Open

Closed

Category PESNet Protocol

Assigned By Jerry Francis

Summary Program the previous implementation of PESNet

Description The PESNet protocol must be programmed in VHDL. It should have an interface to the Cypress communication chip, CY7C9689-AC. The previous phase legs should be able to use this code. The code is available using Altera Design Manager. It is in schematic form, however. It needs to be translated into VHDL. See the PEBB Plug and Play annual report for 2001.

Comments

Assigned To Jerry Francis

T#6

Opened 2/25/2002 3:31:35 PM

Status Closed

Closed 3/5/2002

Category Lab Area

Assigned By Bob Martin

Summary Order special soldering iron tips

Description Order special SMD soldreing iron tips for 0805 packages and 1206 packages. Soldering iron tips should fit on the PES50 soldering irons

Comments Bob Martin, 2/24/2002, (9): Maybe we cannot get the tips for PES50 handle. We may have to get them for the TC201T handle.
Jerry Francis, 3/8/2002, (32): Soldering Iron tips are here, and they seem to work well.

T#12

Opened 2/25/2002 4:52:41 PM

Status Closed

Closed 3/7/2002

Category Lab Area

Assigned By Fred Wang

Summary Make story for Thales visit

Description In particular, please look at the short term plan toward the end of the document. The "story" is what we need to prepare for the next week's meeting. Jerry, please think a little from the controller side. We probably can brainstorm a little bit later this week to formulate the story.

Comments Jerry Francis, 2/28/2002, (19): Started to make power point presentation about all converters and processors used. So far, I have slides.
Fred Wang, 2/28/2002, (16): Dr. Borojevic asked us to focus on the boards we have used for the upcoming Thales project, namely:
1) The 2101 board (quite ole per Dr. B, used extensively in previous projects, Wei Dong might have some idea on it.)
2) The commercial Sharc board
3) The big Sharc you arr using now
Jerry Francis, 3/7/2002, (26): Finished slides and sent them to Dr. Wang. Set task to closed.

T#11

Opened 2/25/2002 4:50:22 PM

Status InProgress

Closed

Category Lab Area

Assigned By Bob Martin

Summary Create plan

Description Need to create a plan to post on the website of what the digital lab coordinator will do.

Comments Jerry Francis, 2/25/2002, (10): Based on the proposal submitted on Feb. 6, 2002

T#27

Opened 3/4/2002 8:48:06 AM

Status Open

Closed

Category Lab Area

Assigned By Bob Martin

Summary Find capacitors for Cornell-Dubilier

Description We get donations from Cornell-Dubilier. Find a list of capacitor reels that we should request from them.

Comments

Project: *Community Service*

Assigned To Haifei Deng

T#7

Opened 2/25/2002 3:35:41 PM

Status InProgress

Closed

Category Software Support

Assigned By Jerry Francis

Summary Common drawing symbols

Description Make common components for power electronics in Powerpoint and Visio, such as inductors, capacitors, resistors, transistors (IGBT, mosfet, eto, scr, . . .) and other appropriate components

Comments Jerry Francis, 2/26/2002, (11): Sent an email to Haifei Deng asking him to do the library.

Haifei Deng, 2/28/2002, (15): I have built some symbols now. However, it is not finished. I will contact with you [Jerry] several days later.

TasksCategoryTotals

AssignedTo	Closed	InProgress	Open	Reopened	Resolved
				0	
Jerry Francis	9	5	5		3
Luca Solero		1			
Xiangfei Ma		1	1		
Jinghong Guo		1			
Haifei Deng		1			
Daniel Ghizoni		1			
Gasha Gataric		1	3		4